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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/716,956	11/19/2003	Alexander B. Hoefler	SC12779TP	6451	
23125	7590 01/05/2005		EXAMINER		
FREESCALE SEMICONDUCTOR, INC.			LE, TH	LE, THAO P	
LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			ART UNIT	PAPER NUMBER	
			2818	- I AI EK NOMBEK	
	, , , , ,		DATE MAILED: 01/05/2009	_	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
Office Action Commons	10/716,956	HOEFLER ET AL.				
Office Action Summary	Examiner	Art Unit				
	Thao P. Le	2818				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 17 No.	ovember 2004.					
2a) This action is <b>FINAL</b> . 2b) ☑ This	_					
3) Since this application is in condition for allowar	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is					
closed in accordance with the practice under E	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4)⊠ Claim(s) <u>1-38</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw	4a) Of the above claim(s) is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-21</u> is/are rejected.	☑ Claim(s) <u>1-21</u> is/are rejected.					
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	r election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10)⊠ The drawing(s) filed on 11/19/03 is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correct						
11)☐ The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>						
Attachment(s)	_					
<ol> <li>Notice of References Cited (PTO-892)</li> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1 page.</li> </ol>	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

#### **DETAILED ACTION**

### Election/Restriction

Examiner confirms that Applicants elected to prosecute Claims 1-21 and have withdrawn Claims 22-38 without prejudice.

#### Information Disclosure Statement

Information Disclosure Statement (IDS) filed on **11/19/03** and made of record.

The references cited on the PTOL 1449 form have been considered.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 4-16, 21 are rejected under 35 USC 102 (a) as being anticipated by Sun et al., U.S. Patent No. 6,630,384.

Regarding claim 1, Sun et al. discloses a method of forming a non-volatile memory similar to what recited in claim 1. See Figs. 2-7 and Cols. 1-12, the method comprising:

providing a semiconductor substrate 112;

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two bit lines defines boundaries and active region disposed between bit lines (Figs. 1-7);

- providing a charge storage layer 114 overlying the substrate;
- forming a first control gate 116 over the charge storage layer, forming an insulating liner 118 over the first control gate;

forming a first and second sidewall spacer 120 on two sides of control gate, the first and second spacer control gates is separated from the control gate by insulating liner, and charge storage regions are created within the charge storage layer beneath control gates.

Regarding claims 4-7, Sun et al. discloses the charge storage layer includes a charge storage stack, and the storage stack includes a bottom insulating layer, charge storage layer, and top insulating layer, the storage stack includes at least a layer consisting of oxynitride, or an ONO stack (stack 14).

Regarding claims 8-9, Sun et al. discloses the at least two buried bit lines includes a plurality of buried bit lines and formed to providing of the charge storage layer (lines 1-15, Col. 6).

Regarding claims 10-11, Sun et al. discloses the control gate includes polysilicon (lines 43-45, Col. 6).

Regarding claim 12, Sun et al. discloses the insulating liner includes oxide (lines 66-67, Col. 6).

Regarding claim 13, Sun et al. discloses the formation of plurality of first control gates and insulating liner formed overlying the plurality of first control gates (Fig. 5).

Regarding claims 14-16, Sun et al. discloses the limitations recited in claims 1416; forming charge storage regions underlying the control gate and sidewall spacer, the first and second spacers are adjacent and separated from control gate by insulating liner

Regarding claim 21, Sun et al. discloses wherein the charge storage regions are programmable via a process of hot carrier injection.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 17-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Sun et al., U.S. Patent No. 6,630,384.

Regarding claims 2-3, Sun et al. fails to discloses the step of providing a protective layer over the charge storage layer and the protective layer is made of nitride. However, it is well known in the art that it is obvious to one having ordinary skill in the art to form a protective layer made of nitride or any insulating material over the storage charge layer in order to add extra insulating and prevent charge leaking/diffusion between the control gate and storage charge layer.

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silicide in order to reduce resistance.

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Regarding claims 17-20, Sun et al. fails to discloses the limitations as applied in claims 17-20, however, it is well known in the art at that a conductive material includes polysilicon can be used to from sidewall spacer and the control gate and spacer are

Gill et al. (U.S. Patent No. 5,023,680) and Eitan et al., (submitted by applicant as prior art) also discloses the limitations recited in present application.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Business Center (EBC) at 866-217-9197 (toll-free).

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

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Thao P. Le Examiner

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